CONTINUOUS INTERNAL EVALUATION- 2

Dept:ECE	Sem / Div:5 ECE	Sub:Verilog HDL	S Code:18EC56
Date: 3-12-2020	Time:2:30 - 4:00PM	Max Marks: 50	Elective:N

Note: Answer any 2 full questions, choosing one full question from each part.

QN		Questions	Marks	RB	COs
		PART A			
1	a	Write a verilog data flow level of abstraction for 4 to 1 multiplexer using conditional operator.	4	L3	CO3
	b	Explain different types of event based timing control	7	L2	CO3
	c	Explain blocking assignment statements with relevant examples.	7	L2	CO3
	d	Explain the gate instantiation of AND/OR gates.	7	L2	CO2
		OR			
2	a	Explain non-blocking assignment statements with relevant examples.	9	L2	CO3
	b	Explain structured procedure statements in Verilog?	10	L2	CO3
	c	What are Rise,Fall and Turnoff delays? How are they specified in Verilog?	6	L2	CO2
		PART B			
3	a	Design 4:1 multiplexer using gate level modeling or structural description. Write stimulus block	9	L3	CO3
	b	Explain conditional if else and loop for statemnts with examples.	10	L2	CO3
	c	Explain different types of delay based timing control?	6	L2	CO3
		OR			
4	a	Write a verilog data flow level of abstraction for full subtractor. Write the stimulus block	9	L3	CO3
	b	What would be the output of the following a=4'bl0l0, b=4'b1111, i)a&b ii)a&&&b iii)&a iv)a>>1 v)a>>>1 vi)y={2{a}} vii) a ^ b viii) z= {a, b}.	8	L3	CO2
	c	Explain level sensitive timing control.	3	L2	CO3
	d	Design a 2-to-1 multiplexer using bufif0 and bufif1 gates as shown in Fig1.Apply stimulus	5	L3	CO2

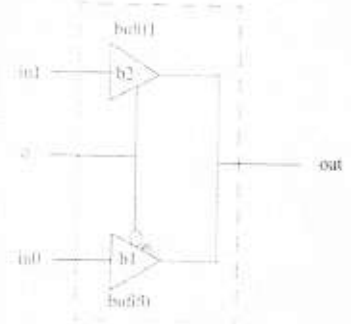

Fig1

	Min	Typ	Max
Rise	1	2	3
Fall	3	4	5
Turnoff	5	6	7

Fig2

The delay specification for gates b1 and b2 is shown in Fig 2

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HOD